Notice of Allowability	Application No. 10/687,124	Applicant(s) FACKENTHAL, RICHARD E.	
	Examiner Guy J. Lamarre	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *07/19/2007*.

2. ☒ The allowed claim(s) is/are *1-4, 6-18, 20-30, 32-39, 41-48; now renumbered 1-44*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *10/26/07* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Guy J. Lamarre, P.E
Primary Examiner

Examiner's Amendment & Reasons For Allowance

* **Claims 1-48** are pending.

* The rejections of record to **Claims 1-48** are withdrawn in response to Applicants' **Appeal Brief**.

* The Examiner gratefully acknowledges Applicants' cooperation in expediting prosecution of instant application.

Examiner's Amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The following has been amended as follows:

a. **Claims 5, 19, 31, 40** are cancelled.

b. The claims are as listed below:

1. A method comprising:

selectively storing data in a memory array at different densities per cell; and

implementing error correction depending on the density of data storage; wherein implementing error correction depending on the density of data storage includes determining whether data is in a higher or lower density mode; and

if the data is in a higher density mode, implementing error correction code; and

if the data is in a lower density mode, omitting error correction code.

2. The method of claim 1 including selectively storing data in a memory at different densities per cell by using different numbers of threshold voltage levels in a given cell.

3. The method of claim 2 including using a higher density mode with double the number of threshold levels as a lower density mode.

4. The method of claim 3 including using a higher density mode with four threshold levels and a lower density mode using two threshold levels.

5. **(cancelled.)**

6. The method of claim **1** including using a flag to indicate whether or not the data is in a lower or higher density mode.

7. The method of claim **1** including allowing overwriting when the data is stored in the lower density mode.

8. The method of claim 7 including preventing overwriting when the data is stored in the higher density mode.

9. The method of claim 1 including allowing overwriting of stored data when error correcting codes are not provided for that data.

10. The method of claim 1 including providing a multi-level memory cell array having a capacity of at least four levels.

11. The method of claim 10 including using at least two bits to represent said at least four levels.

12. The method of claim 11 including using one of said bits as a more significant bit and the other of said bits as a less significant bit.

13. The method of claim 12 wherein data from at least two cells forms a codeword and grouping the more significant bits from different cells together.

14. The method of claim 13 including providing more significant bits in one half of a word and less significant bits in the other half of a word.

15. An article comprising a medium storing instructions that, if executed, enable a processor-based system to:

selectively store data in a memory array at different densities per cell; and

implement error correction depending on the density of data storage;

wherein to implement error correction depending on the density of data storage includes determining whether data is in a higher or lower density mode; and

if the data is in a higher density mode, implement error correction; and

if the data is in a lower density mode, omit error correction.

16. The article of claim 15 further storing instructions that, if executed, enable the system to selectively store data in a memory at different densities per cell by using different numbers of threshold voltage levels in a given cell.

17. The article of claim 16 further storing instructions that, if executed, enable the system to use a higher density mode with double the number of threshold levels as a lower density mode.

18. The article of claim 17 further storing instructions that, if executed, enable the system to use a higher density mode with four threshold levels and a lower density mode using two threshold levels.

19. (cancelled.)

20. The article of claim 15 further storing instructions that, if executed, enable the system to use a flag to indicate whether or not the data is in a lower or higher density mode.

21. The article of claim 15 further storing instructions that, if executed, enable the system to allow overwriting when the data is stored in a higher density mode.

22. The article of claim 20 further storing instructions that, if executed, enable the system to prevent overwriting when data is stored in the higher density mode.

23. The article of claim 15 further storing instructions that, if executed, enable the system to allow overwriting of stored data when error correcting codes are not provided for that data.

24. The article of claim 15 further storing instructions that, if executed, enable the system to provide a multi-level memory cell array having a capacity of at least four levels.

25. The article of claim 24 further storing instructions that, if executed, enable the system to use at least two bits to represent said at least four levels.

26. The article of claim 25 further storing instructions that, if executed, enable the system to use one of said bits as a more significant bit and the other of said bits as a less significant bit.

27. The article of claim 26 wherein data from at least two cells forms a codeword and further storing instructions that, if executed, enable the system to group the more significant bits from different cells together.

28. The article of claim 27 further storing instructions that, if executed, enable the system to provide more significant bits in one half of a codeword and less significant bits in the other half of a codeword.

29. A memory comprising:

a memory array; and

a controller coupled to said memory array to selectively store data in the memory array at different densities per cell and to implement error correction depending on the density of data storage;

wherein said controller to determine whether data is in a higher or lower density mode and if the data is in a higher density mode, implements error correction and if the data is in a lower density mode, omits error correction.

30. The memory of claim 29 wherein said memory array is a multi-level flash memory array.

31. (cancelled.)

32. The memory of claim 29 said controller to allow overwriting when the data is stored in the lower density mode.

33. The memory of claim 32 said controller to prevent overwriting when the data is stored in the higher density mode.

34. The memory of claim 29 said controller to allow overwriting of stored data when error correcting code is not provided for that data.

35. The memory of claim 29 said controller to use at least two bits to represent four threshold voltage levels.

36. The memory of claim 35 said controller to use one of said bits as a more significant bit and the other of said bits as a less significant bit.

37. The memory of claim 36 said controller to group the more significant bits from different cells together.

38. A system comprising:

a processor;

a wireless interface; a memory coupled to said processor; and

a controller coupled to said memory to selectively store data in said memory at different densities per cell and to implement error correction depending on a density of data storage;

wherein said controller to determine whether data is in a higher or lower density mode and if the data is in a higher density mode, implements error correction and if the data is in a lower density mode, omits error correction.

39. The system of claim 38 wherein said memory is a multi-level flash memory.

40. (cancelled.)

41. The system of claim **38** said controller to allow overwriting when the data is stored in the lower density mode.

42. The system of claim 41 said controller to prevent overwriting when the data is stored in the higher density mode.

43. The system of claim 38 said controller to allow overwriting of stored when error correcting codes are not provided for that data.

44. The system of claim 38 said controller to use at least two bits to represent four threshold levels.

45. The system of claim 44 said controller to use one of said bits as a more significant bit and the other said bits as a less significant bit.

46. The system of claim 45 said controller to group the more significant bits from different cells together.

47. The system of claim 38 wherein said wireless interface includes an antenna.

48. The system of claim 47 wherein said wireless interface includes a dipole antenna.

Reasons For Allowance

2. **Claims 1-4, 6-18, 20-30, 32-39, 41-48** thus remain pending.

.1 Applicants' arguments of 7/19/07 along with the entire disclosure have been fully considered and are found persuasive. As a result, **Claims 1-4, 6-18, 20-30, 32-39, 41-48.**

.2 **Claims 1-4, 6-18, 20-30, 32-39, 41-48** are allowable over the prior art. The following is an examiner's statement of reasons for allowance:

The prior art of record, as exemplified by **Gregori** ("*Construction of Polyvalent Error Control Codes for Multilevel Memories*," pp. 751-754, IEEE, 2000), does not teach or suggest alone or in combination '*implementing error correction depending on the density of data storage includes determining whether data is in a higher or lower density mode; and if the data is in a higher density mode, implementing error correction code; and if the data is in a lower density mode, omitting error correction code.*'

.3 Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

* Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (571) 273-8300 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached at (571) 272-6962.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner